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Semiconductor Processing Methods Of Forming Integrated Circuitry

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SEMICONDUCTOR PROCESSING METHODS OF FORMING INTEGRATED CIRCUITRY

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TECHNICAL FIELD

This invention relates generally to semiconductor processing methods of forming integrated circuitry, and particularly to methods of forming integrated circuit devices having different threshold voltages.

BACKGROUND OF THE INVENTION

Field effect transistors are characterized by a source region, a drain region and a gate. The source and drain regions are typically received within a semiconductive material, such as a semiconductive substrate. The gate is typically disposed elevationally over the source and drain regions. A gate voltage of sufficient minimum magnitude can be placed on the gate to induce a channel region underneath the gate and between the source and drain regions. Such channel-inducing voltage is typically referred to as the transistor's threshold voltage, or V_t. Accordingly, the threshold voltage turns the transistor on. Once the magnitude of the threshold voltage has been exceeded, current can flow between the source and drain regions in accordance with a voltage called the source/drain voltage, or V_{ds}.

Threshold voltage magnitudes can be affected by channel implants. Specifically, during fabrication of semiconductor devices, a substrate can be implanted with certain types of impurity to modify or change the

threshold voltage of a resultant device. Such channel implants can also affect a condition known as subsurface punchthrough. Punchthrough is a phenomenon which is associated with a merging of the source and drain depletion regions within a MOSFET. Specifically, as the channel gets shorter (as device dimensions get smaller), depletion region edges get closer together. When the channel length is decreased to roughly the sum of the two junction depletion widths, punchthrough is established. Punchthrough is an undesired effect in MOSFETS.

One way of addressing punchthrough in sub-micron devices is through provision of a so-called halo implant, also known as a "pocket" implant. Halo implants are formed by implanting dopants (opposite in type to that of the source and drain) within the substrate proximate the source and drain regions, and are typically disposed underneath the channel region. The implanted halo dopant raises the doping concentration only on the inside walls of the source/drain junctions, so that the channel length can be decreased without needing to use a higher doped substrate. That is, punchthrough does not set in until a shorter channel length because of the halo.

It is desirable to have MOSFETS with different threshold voltages depending upon the context in which the integrated circuitry of which they comprise a part is to be used. In the context of memory devices it can be beneficial to have transistors with different threshold voltages.

This invention arose out of concerns associated with improving the methods through which integrated circuits are fabricated. In particular, the invention arose concerns associated with providing improved methods of forming memory devices.

SUMMARY OF THE INVENTION

Semiconductor processing methods of forming integrated circuitry are described. In one embodiment, memory circuitry and peripheral circuitry are formed over a substrate. The peripheral circuitry comprises first and second type MOS transistors. Second type halo implants are conducted into the first type MOS transistors in less than all of the peripheral MOS transistors of the first type. In another embodiment, a plurality of n-type transistor devices are formed over a substrate and comprise memory array circuitry and peripheral circuitry. At least some of the individual peripheral circuitry n-type transistor devices are partially masked, and a halo implant is conducted for unmasked portions of the partially masked peripheral circuitry n-type transistor devices. In yet another embodiment, at least a portion of only one of the source and drain regions is masked, and at least a portion of the other of the source and drains regions is exposed for at least some of the peripheral circuitry n-type transistor devices. A halo implant is conducted relative to the exposed portions of the source and drain regions. In another embodiment, a common masking step is used and a halo implant is

conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment in process, which is suitable for use in connection with one or more embodiments of the present invention.

Fig. 2 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 3 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 4 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 5 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 6 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 7 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment in process is shown generally at 10 and includes a semiconductive substrate 12. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Memory array circuitry 14 and peripheral circuitry 16 are formed over substrate 12. Memory circuitry 14 comprises individual transistors 20, 22. Peripheral circuitry 16 comprises a transistor 26. These transistors are shown for example only. Each exemplary transistor will typically include a conductive gate line 28 (designated for transistors 20 and 26 only) having a gate oxide layer 30, a polysilicon layer 32, a silicide layer 34, and an overlying insulative cap 36. Conventional sidewall spacers SS are optionally provided over the sidewalls of gate

line 28. Of course, other gate line constructions could be used. Source/drain regions 37 and 38 are provided within substrate 12.

The drain regions 37 may be formed in several different ways. In one embodiment, the drain regions 37 are doped first with a blanket n-minus implant, which may be performed before or after formation of the sidewalls SS. As used herein, the term "blanket implant" refers to an implant process that does not employ a masking step. In one embodiment, the drain regions 37 are doped by out-diffusion of dopants from a doped polysilicon layer forming a portion of a storage node 39.

The source regions 38 may also be formed in several different ways. In one embodiment, the source regions are doped first with a blanket n-minus implant 37' and then with a n-plus implant, followed by a halo implant 41.

Typically, the transistors forming peripheral circuitry 16 will include first- and second-type MOS transistors. For example and for purposes of the on-going discussion, first-type MOS transistors will comprise n-type transistors, and second-type MOS transistors will comprise p-type transistors. Similarly, in this example, implants comprising a second-type of material will comprise p-type implants such as boron.

Referring to Fig. 2 and 3, a masking layer 40 is formed over substrate 12. Transistor 42 (Fig. 2) can constitute a transistor which is disposed within the memory array, or one which is disposed within the peripheral area. Similarly, transistor 26 (Fig. 3) can constitute a

transistor which is disposed within the memory array, or one which is disposed within the peripheral area. Transistor 26 can represent one of many similar partially-masked transistors in either the peripheral area or the memory array. In one embodiment, and with masking layer 40 in place, a second-type halo implant is conducted into transistor 26 and in less than all transistors of the first type. The halo implant forms a halo region 41 received within substrate 12. In this case, transistor 42 can constitute a transistor which does not receive the halo implant. In one embodiment, when transistors receive the halo implant, only one side of the transistor receives the implant, such as shown in Fig. 3. This constitutes a different transistor having a different threshold voltage V_t than those transistors not receiving the halo implant.

Specifically, in one embodiment, transistor 26 comprises an n-type transistor device which is partially masked, and the halo implant is conducted for unmasked portions of the transistor or transistors. Various portions of transistor 26 can be masked to result in a partially masked transistor. For example, at least a portion of one of the source and drain regions can be masked, and at least a portion of the other of the source and drain regions can be exposed. As a further example, a majority portion of one of the drain regions can be masked, while a majority portion of the other of the source regions is not masked for at least some of the devices. In the illustrated example, an entirety of one of the drain regions is masked, and the entirety of the other of the

source regions is not masked. Where a transistor's source region is masked, after the halo implantation, the transistor will have a configuration similar to a source follower configuration. Where a transistor's drain region is masked, after the halo implantation, the transistor can have its electric field suppressed proximate the drain.

In another embodiment, the second-type halo implants are conducted into only one of the source and drain regions in less than all of the MOS transistors of the first type, and not the other of the source and drain regions of those peripheral MOS transistors of the first type.

Referring to Fig. 4, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. Rightmost transistor 26a has both source and drain regions masked, and constitutes other n-type transistor devices which do not receive a halo implant. As a result, the rightmost transistor 26a has a lower threshold voltage V_t than transistors receiving the halo implant.

Referring to Fig. 5, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. Transistor 26b has both of its source and drain regions left exposed during the halo implant. Accordingly, halo regions 41 are formed proximate the source/drain regions of transistor 26b.

Referring to Fig. 6, another embodiment of the invention is shown. Leftmost transistor 26 can comprise any of the partially-masked configurations described with respect to Fig. 3. In this embodiment, portions of transistors in either the peripheral or the memory array region are partially masked, and, in addition, the source regions and drain regions for some other individual transistor devices are masked, e.g. transistor 26a, while different other individual peripheral transistor devices, e.g. transistor 26b, have their source regions and drain regions exposed during the halo implant. Accordingly, where both of the source and drain regions are exposed, a pair of halo regions 41 is formed. These associated transistor devices having both source and drain regions exposed are, for purposes of this document, referred to as first transistor devices. Where both of the source and drain regions are masked or otherwise blocked, no halo regions are formed. These associated transistor devices having both source and drain regions masked or blocked are, for purposes of this document, referred to as second transistor devices. Where a portion of a transistor device is exposed, a halo region can, in some instances, be formed with respect to only one of the source and drain regions. These associated transistor devices are, for purposes of this document, referred to as third transistor devices. Preferably, these associated transistor devices are all NMOS transistor devices.

Alternately considered, and in a preferred embodiment, a common masking step is utilized and in a common implant step, a halo implant is conducted of devices formed over a substrate comprising memory circuitry and peripheral circuitry, sufficient to impart to at least three of the devices three different respective threshold voltages. In one embodiment, the three devices comprise NMOS field effect transistors.

In the context of NMOS field effect transistors in which the implanted halo impurity comprises a p-type impurity, those transistors whose source and drain regions are fully exposed, will typically have the highest threshold voltage V_{t1}. Those transistors which are partially masked during the halo implant will typically have a threshold voltage V_{t2} which is somewhat lower than threshold voltage V_{t1}. Those transistors whose source and drain regions are completely blocked during the halo implant will typically have the lowest threshold voltage V_{t3} of the threshold voltages. Accordingly, three different threshold voltages are provided through one common masking step.

Fig. 7 is a side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the invention. Transistors 20 and 22 of Fig. 1 now form memory access transistors 45 having a threshold voltage that corresponds to a single halo implant 41 on a bitline contact side of the access transistors 45. Storage node sides 47 of the access transistors 45 are masked by the masking layer 40 to prevent boron from being implanted. Forming access transistors

45 in this way improves refresh capabilities. The one-sided halo implant 41 in the access transistors 45 allows the channel doping to be reduced while maintaining the same threshold voltage V_t and subthreshold voltage. The lower channel doping, in turn, gives rise to improved DRAM refresh characteristics, because charge leakage from the storage nodes 47 is reduced.

It will be appreciated that the halo implant and the mask 40 therefor may be effectuated before formation of sidewall spacers (denoted "SS" in Fig. 1), as shown in Figs. 2-7, or after formation of sidewall spacers (as shown in Fig. 1). The sidewall spacers SS shown in Fig. 1 may be formed using conventional deposition, oxidation and/or etching techniques. It will be appreciated that when boron is implanted into a n-type device, n-well bias plugs and other conventional features should be masked to avoid compromise of the conductivity of these features.

When the halo implant is done with a mask, prior to formation of sidewall spacers SS, it is normally accompanied by an n-minus implant 37, using either phosphorous or arsenic. When the halo implant is done after formation of the sidewall spacers SS, it is assumed that the n-minus layer 37 was formed earlier as part of a LDD (lightly doped drain) structure. This same halo implant is normally accompanied by an n+ source drain implantation.

One preferred application for such devices can be in the context of peripheral circuitry comprising a so-called equilibrating device, which is typically connected between bit lines D and D* in dynamic random access memory circuitry in order to bring the bit lines to a common voltage potential (typically $V_{cc}/2$) prior to firing the word lines to perform a sensing operation. Another application can be for the cross-coupled transistors in a sense amplifier circuit, where lower threshold voltage V_t is preferred for better margin and refresh properties. Other applications can include various low-voltage applications which will be apparent to the skilled artisan.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.